Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit, comprising:

at least one processing unit (PU);

a cache memory (L2_bank) having a plurality of memory modules for caching data, wherein the cache memory comprises a plurality of distinct physical banks, wherein each physical bank comprises some of the memory modules and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks; and

signal selection circuitry for identifying which data cached in said cache memory, wherein the signal selection circuitry comprises:

a Tag RAM unit (TagRAM) to generate a hit signal based on an input address, wherein the hit signal is indicative of an originally mapped way for data corresponding to the input address; and

remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules, wherein the remapping means is configured to generate a hit' signal based on the hit signal from the Tag RAM unit, wherein the hit' signal is indicative a remapped way for the data corresponding to the input address.

2. (previously presented) The integrated circuit according to claim 1, wherein said cache memory (L2_BANK) is a set-associative cache.

3. (previously presented) The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.

4. (previously presented) The integrated circuit according to claim 1, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping, wherein the reduction mapping performs the remapping using less output symbols than input symbols.

5. (currently amended) The integrated circuit according to claim 1, further comprising:

~~a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and~~

wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM) to receive the hit signal from the Tag RAM unit for use in generating the hit' signal indicative of the remapped way.

6. (currently amended) The integrated circuit according to claim 1, further comprising:

~~a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2_BANK), and~~

wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM) to generate a plurality of remapped banks and ways corresponding to the input address, wherein the remapped banks and ways corresponding to the input address are generated independently of the hit signal from the Tag RAM unit and are subsequently processed together with the hit signal from the Tag RAM unit by selection logic to generate the hit' signal indicative of the remapped way.

7. (previously presented) The integrated circuit according to claim 5, further comprising:

a look up table for marking faulty memory modules.

8. (currently amended) A method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing data; and a cache memory (L2_BANK) having a plurality of memory modules for caching data, the method comprising:

generating a hit signal based on an input address, wherein the hit signal is indicative of an originally mapped way for data corresponding to the input address;

performing an unrestricted remapping within said plurality of memory modules, wherein the memory modules are distributed among a plurality of distinct physical banks within the cache memory, and each physical bank is configured to facilitate serving a read/write request independently of the other physical banks to allow concurrent transfers for at least two of the physical banks, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules; and

generating a hit' signal based on the hit signal, wherein the hit' signal is indicative a remapped way for the data corresponding to the input address.

9. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to distribute faulty memory modules evenly over a plurality of banks.

10. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to perform the unrestricted remapping at a block/line granularity of the memory modules.

11. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules.

12. (previously presented) The integrated circuit according to claim 1, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

13. (previously presented) The integrated circuit according to claim 1, wherein the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

14. (previously presented) The method of cache remapping according to claim 8, further comprising performing the unrestricted remapping on the basis of a reduction mapping using less output symbols than input symbols.

15. (previously presented) The method of cache remapping according to claim 8, further comprising marking faulty memory modules in a look up table.

16. (previously presented) The method of cache remapping according to claim 8, wherein said cache memory comprises a plurality of dynamic random access memory (DRAM) modules.

17. (previously presented) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a same index within the second physical bank of memory modules.

18. (previously presented) The method of cache remapping according to claim 8, further comprising remapping at least one of the memory modules to a new way and a different index within the second physical bank of memory modules.

19. (previously presented) The integrated circuit according to claim 1, wherein each physical bank of memory modules is located on a separate DRAM module.

20. (previously presented) The method of cache remapping according to claim 8, wherein each physical bank of memory modules is located on a separate DRAM module.